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Applicant(s): In-Jung Lee, et al.
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Title: CAPACITOR AND FABRICATING METHOD THEREFOR

Examiner: Nguyen, C.
Group Art Unit: 2811

CERTIFICATE OF MAILING UNDER 37 C.F.R. 1.8

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APPEAL BRIEF

Sir:

This is an Appeal Brief in regard to the final rejection of the claims in the above-identified patent application set forth in the final Office Action mailed on June 20, 2003. A Notice of Appeal was transmitted by facsimile to the United States Patent and Trademark Office on September 22, 2003. This brief is being filed in triplicate as required by 37 C.F.R. §1.192. The $330.00 fee for filing a brief in support of an appeal under 37 C.F.R. §1.17(c) is enclosed. Also enclosed is a fee of $950.00 as payment for the fee for a three-month extension of time.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 50-1798. A duplicate copy of this letter is provided for this purpose.

I. Real Party In Interest

The real party in interest is Samsung Electronics Co., Ltd., a corporation of the Republic of Korea.

II. Related Appeals and Interferences

There are no directly related appeals or interferences regarding this application.

III. Status of Claims

Claims 1-3, 5 and 6 are pending in this Application. Claim 4 is canceled. Claims 7-13 have been withdrawn as being directed to a non-elected invention. Claims 1-3, 5 and 6 have been finally rejected. The rejections of Claims 1-3, 5 and 6 are appealed.

IV. Status of Amendments

An Amendment After Appeal is submitted herewith. In the Amendment, claim 5 is amended to depend from claim 1 instead of claim 4, claim 4 having been canceled previously. Entry of the Amendment After Appeal is requested.

The applicants filed a Response to the final Office Action on August 20, 2003, but that Response contained no amendments. In the Advisory Action mailed on September 10, 2003, is it indicated that the Response mailed on August 20, 2003 is entered.

Upon entry of the enclosed Amendment After Appeal, the present state of the claims will be in accordance with the listing of the claims contained in the Appendix hereto.

V. Summary of the Invention

The invention relates to a semiconductor wire-bond attached chip capacitor (WACC). Referring to Figure 2d of the application and the description of the invention in the specification as filed, at least at page 6 line 22 through page 9 line 4, the WACC of the invention includes a lower electrode II, an upper electrode I and a capacitor dielectric layer 104, 112. The upper electrode I includes a polysilicon pattern 106', and a blocking metal layer pattern is formed on top of the polysilicon pattern 106'. The polysilicon pattern 106' is formed of a three-layer polysilicon deposition structure, which includes a

lower first undoped polysilicon layer 106a, a middle second doped polysilicon layer 106b and an upper third undoped polysilicon layer 106c. A metal blocking layer is formed over the upper undoped polysilicon layer 106c to form a first metal pattern 110a connected to the upper undoped polysilicon layer 106c to complete the formation of the upper electrode I.

The upper undoped polysilicon layer 106c is used in the WACC of the invention to provide the interface to the metal pattern 110a to provide a thicker adhesion layer between the metal pattern 110a and the polysilicon pattern 106'. This prevents lifting of the metal pattern 110a from the polysilicon pattern 106'. Adhesion is important in the semiconductor WACC because the WACC is coupled to other circuits by wiring bond pads positioned between the circuit components and the WACC.

VI. Issues

Whether Claims 1-3 are unpatentable under 35 U.S.C. §103(a) as being obvious over what is referred to as the Admitted Prior Art (APA) of Figure 1d of the application in view of Chen, *et al.* (U.S. Patent Number 6,033,950).

Whether Claims 5 and 6 unpatentable under 35 U.S.C. §103(a) as being obvious over the APA in view of Chen, *et al.* and further in view of Hanagasaki (U.S. Patent Number 5,767,541).

VII. Grouping of Claims

The claims stand or fall together. There is one group of claims, which includes claims 1-3, 5 and 6.

VIII. Argument

A. Claims 1-3

Claims 1-3 are rejected under 35 U.S.C. §103(a) as being unpatentable over what is referred to as the Admitted Prior Art (APA) of Figure 1d of the application in view of Chen, *et al.* (U.S. Patent Number 6,033,950).

With regard to the APA, the structure illustrated in Figure 1d of the application and described in the applicants' Background of the Invention section, the polysilicon

pattern in the capacitor electrode is a two-layer pattern which includes a lower undoped polysilicon layer and an upper doped polysilicon layer. A metal pattern is formed over the upper doped polysilicon layer. During subsequent processes such as an annealing process, a silicide layer is formed between the polysilicon layer and the metal pattern, resulting in adhesion between the metal layer and the polysilicon. Adhesion between the silicon and the metal layer is determined by the degree to which the metal and silicon react during annealing. The thickness of the resulting silicide layer is inversely related to the doping concentration in the layer of polysilicon in contact with the metal layer. Thus, the high impurity concentration in the polysilicon layer of the APA of Figure 1d results in a relatively thin silicide layer, which, in turn, results in relatively poor adhesion between the metal and the polysilicon.

Hence, the applicants' improvement over the prior art device involves reducing the impurities in the layer contacting the metal. This results in a thicker layer being formed between the two during the annealing process, which results in better adhesion.

In Chen, *et al.*, an undoped polysilicon layer 34 is formed on a doped polysilicon layer 32 to form an electrode of a capacitor. The undoped layer 34 is covered by an insulating layer 40. The upper undoped polysilicon layer 34 is used to reduce out-diffusion of impurities from the lower doped polysilicon during thermal cycles, thus preventing auto doping. In auto doping, the dopant diffuses out of the polysilicon and reaches the surface of the device and diffuses into the substrate during subsequent thermal processes. In other devices formed on the same wafer, the out-diffused dopant laterally and vertically increase the other dopant concentrations near or under edges of channel regions of adjacent devices. The undoped polysilicon layer 34 is placed on top of the doped polysilicon layer 32 to prevent this out-diffusion of dopant.

Claims1-3 are not unpatentable under 35 U.S.C. §103(a) over the APA of Figure 1d of the application and Chen, *et al.* One of skill in the art would not be motivated to make the cited combination, and, even if the combination were made, it does not result in the claimed invention.

To establish a prima facie case of obviousness, the prior art reference or references when combined must not only teach or suggest all the recitations of the claim, there must also be some suggestion or motivation, either in the references themselves or

in the knowledge generally available to one of ordinary skill in the art, to modify the reference themselves or to combine reference teachings. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). To support combining references, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement for clear and particular evidence is not met by broad and conclusory statements about the teachings of the reference. In re Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. To support combining or modifying references, there must be particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. In re Rouffet, 149 F.3d at 1357, 47 USPQ2d at 1456; see also In re Werner Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). A reference must provide some motivation or reason for one skilled in the art, working without the benefit of the applicants' specification, to make the necessary changes in the disclosed device. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The mere fact that a reference may be modified in the direction of the claimed invention does not make the modification obvious unless the reference expressly or impliedly teaches or suggests the desirability of the modification. In re Gordon, 221 USPQ 1125,1127 (Fed. Cir. 1984); Ex parte Clapp, 227 USPQ 972, 973 (Bd, App. 1985); Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd, App. 1984).

The cited rejections fail to meet the basic requirements for a finding of obviousness. There is no suggestion in the cited references of modifying the device structures disclosed therein in the direction of the present invention, nor is there any suggestion whatsoever of the desirability of such modification.

The claimed invention is directed to the specific requirements of a WACC. Specifically, the upper electrode of the wire-bond attached chip capacitor of the invention has a polysilicon layer constructed in a three-layer deposition structure of a doped polysilicon layer between two undoped polysilicon layers. This results in effective formation of a silicide layer between the polysilicon layer and a blocking metal layer to

reinforce adhesion and to prevent lifting between the layers. This enhancement is specifically directed to the WACC because of the special requirements of the WACC with regard to the prevention of lifting. Hence, the application of the three-layer polysilicon upper electrode structure to the WACC is specific to a WACC and provides that particular structure with the desirable enhancements of the invention.

In the context of the claimed invention, that is, in the context of a WACC structure, there would be no motivation of one of skill in the art to combine the two-layer polysilicon structure of the WACC of the APA of Figure 1d with the two-layer polysilicon structure of Chen, *et al.* Chen, *et al.* use an undoped polysilicon layer on a doped polysilicon layer to prevent out-diffusion from the lower doped polysilicon layer. However, there is no teaching or suggestion in either Chen, *et al.* or the applicants' prior art of any motivation for combining the two-layer structure of Chen, *et al.* with the two-layer structure of the prior art. Particularly, there is no teaching or suggestion in either reference of making such a combination to prevent out-diffusion, for example, or for any other reason. Prevention of out-diffusion is a consideration in the Chen, *et al.* structure because Chen, *et al.* teaches a mixed-mode product, i.e., a product having a capacitor and PMOS devices. As a result, in Chen, *et al.* , prevention of out-diffusion is disclosed as an important feature to prevent auto-doping of the PMOS channel region such that the PMOS devices are not compromised by the out-diffusion. In contrast, there is no teaching or suggestion of such considerations in the applicants' prior art. This is to be expected to one of skill in the art because the APA is directed to a WACC. In the context of that disclosure, there is no suggestion whatsoever in the description of the APA of any consideration of importance of out-diffusion.

Both the applicants' APA device and the device of Chen, *et al.* include two-layer deposition structures. The Chen, *et al.* structure is a two-layer structure with undoped polysilicon over doped polysilicon. The applicants' admitted prior art device is a two-layer structure with undoped polysilicon over doped polysilicon and a metal pattern over the two-layer structure. There is no suggestion in either reference of three-layer structures or any possible benefit to a three-layer structure. Also, Chen, *et al.* does not at all contemplate adhesion of a metal layer, since the undoped polysilicon layer of Chen, *et al.* is adjacent to a thick insulating layer 40, not a metal conductive layer.

The Examiner asserts that one of skill in the art would be motivated to make the combination to prevent out-diffusion. As noted above, the references provide no teaching or suggestion, either implied or explicit, of such a motivation. The Examiner has also not pointed out where such motivations can be found, other than in the unsupported conclusory statement that such motivation exists.

Hence, contrary to the Examiner's statement that the person of skill in the art would be motivated to make the combination to prevent out-diffusion, there is no teaching or suggestion in either reference of such a motivation. The description of a WACC in the APA makes no reference to out-diffusion, and there is nothing in the disclosure of the APA which would allow any inference of such a motivation. In the absence of some explicit teaching in the references of a motivation to combine them, a rejection based on the combination is improper.

Even if the cited combination of the APA and Chen *et al.* were made, the claimed invention would not result.

Attention is directed to the fact that the claimed invention is directed to the combination of the three layers, not to any specific individual layer or pair of layers. That is, the invention is directed to the three-layer structure explicitly set forth in the claims. It is not directed to the single undoped polysilicon layer 106c or to the combination of the undoped polysilicon layer 106c and the doped polysilicon layer 106b. The invention is instead directed to a specific three-layer structure disposed between a dielectric layer and a first metal pattern.

The main feature of claim 1 of the present application, namely, the deposition structure including three layers including a doped polysilicon layer between first and second undoped polysilicon layers, formed on a dielectric layer, with a first metal pattern formed over the electrode, is not needed in the structure of Chen, *et al.*, since such a deposition structure cannot be used in the Chen, *et al.* capacitor structure in which the undoped polysilicon layer 34 is covered by a thick insulating layer 40, not by a metal layer such as the metal layer 110 of the present invention.

The Examiner correctly states that Chen discloses a capacitor structure comprising an upper electrode that includes an undoped polysilicon layer 34. However, it appears that the Examiner assumes that only the undoped polysilicon layer 106c in the

present invention, which corresponds to the undoped polysilicon layer 34 of Chen, is the applicant's claimed invention, and, therefore, by simply inserting the single undoped polysilicon layer 34 of Chen, et al. into the structure of the APA, the claimed invention results. The applicants do not agree with that assumption. The invention in the present case is the complete combination of an upper electrode (I), which comprises a doped polysilicon layer 106b formed between a first undoped polysilicon layer 106a and a second polysilicon layer 106c, and a metal pattern 110a formed deposited over the second undoped polysilicon layer 106c of the upper electrode (I). When taken as a whole, the invention is the combination of the layers, i.e., the upper and lower electrodes and the dielectric therebetween. One of the layers, namely, the upper electrode, includes the claimed composite layer under a metal layer used to make contact with the device. The combination of the structure of Chen, et al. with the APA does not form the structure of the invention, when considered as a whole.

Moreover, the deposition structure of the applicants' claimed invention cannot be used in the capacitor structure of Chen *et al.* in which the undoped polysilicon layer 34 is covered by a thick insulating layer 40, not by a metal layer such as the metal layer 110a of the present invention. The three-layer deposition structure of the present invention is covered by the metal layer 110a, which, in accordance with the present invention, leads to the use of the applicants' undoped polysilicon layer as the polysilicon layer contacting the blocking metal layer, thus reinforcing adhesion and preventing occurrence of lifting therebetween. In addition, the deposition structure of the claimed invention cannot be used on the bottom plate electrode 27 of the Chen, *et al.* device.

Additionally, the three layered polysilicon deposition structure 106' in the present invention is different in its function and effect from that of the undoped polysilicon layer in Chen, *et al.* Specifically, in the present invention the metal layer 110a is formed on the undoped layer 106c, while in Chen, an insulating layer 40 is formed on the undoped polysilicon layer 34. The function in the present invention of the interface between the metal layer 110a and the undoped layer 106c is to reinforce adhesion and prevent the occurrence of lifting therebetween. While in Chen, *et al.*, the function of the interface between the insulating layer 40 and the undoped layer 34 is to prevent out-diffusion from the lower doped polysilicon layer during thermal cycles.

Thus, even if the skilled artisan would be motivated to combine the APA with Chen, *et al.*, the claimed invention does not result.

In summary, the person of skill in the art would not be motivated to combine the APA with Chen, *et al.* Even if the combination were to be made, the claimed invention does not result.

For these reasons, it is believed that claims 1 through 3 are not unpatentable over the APA and Chen, *et al.* under 35 U.S.C. §103(a).

B. Claims 5 and 6

Claims 5 and 6 incorporate claims 1 through 3 by dependency. The above comments with regard to the rejections of claims 1 through 3 apply equally to the rejections of claims 5 and 6.

As discussed above, the combination of the APA and Chen, *et al.* is improper. Accordingly, for the same reasons, the combination of the APA, Chen, *et al.* and Hanagasaki is also improper. Accordingly, it is believed that claims 5 and 6 are not unpatentable over the APA, Chen, *et al.* and Hanagasaki under 35 U.S.C. §103(a).

IX. Conclusion

In view of the arguments presented above, claims 1 through 3 are not unpatentable over the APA and Chen, *et al.* under 35 U.S.C. §103(a). Also, claims 5 and 6 are not unpatentable over the APA, Chen, *et al.* and Hanagasaki under 35 U.S.C. §103(a).

It is respectfully requested that the Examiner's rejections of Claims 1-3, 5 and 6 as being obvious under 35 U.S.C. §103(a) be reversed.

Respectfully submitted,

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APPENDIX

REJECTED CLAIMS

1. A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including three layers including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer, and a first metal pattern formed deposited over the upper electrode, wherein the semiconductor capacitor is a wire-bond attached chip capacitor.

2. The capacitor, as defined in claim 1, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.

3. The capacitor, as defined in claim 1, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.

5. The capacitor, as defined in claim 1, wherein the metal pattern is constructed in a deposition structure including a blocking metal layer and an aluminum layer.

6. The capacitor, as defined in claim 5, wherein the blocking metal layer is constructed in a structure including a Ti layer and a TiN layer.